Performance Enhancement For Spiral Indcutors, Design And Modeling

Mohammad Hossein Nemati

16311

Sabanci University

Final Report for Semiconductor Process course

Introduction:

How to practically improve the inductance of on-chip spiral inductor is always an important research topic in the development of radio frequency integrated circuitry (RFIC) technology. An inductance enhancement scheme can not only reduce chip area occupied by the inductors for low manufacturing cost but also strengthen Q performance of the inductors for high-performance RFIC applications. The Q performance is associated with the signal transmission loss in an on-chip inductor, including the induced eddy current loss originated from the substrate un-demeath itself and the resistive loss coming from the structure material, aluminum or copper. In general, loss reduction can be realized using micromachined technique to fabricate a cav-ity under the coil to reduce the eddy current loss and utilizing connected metal lines by metal via to increase coil conductance. Since the size of inductor can be shrunk via the incorporation of ferromagnetic material, higher Q performance of inductor can be further driven with less eddy current and resistive losses.

Important parameters of inductor are inductance value, self resonance frequency, quality factor. A very simple model for inductor is as follow.



Fig. 1 Simple Lumped model for Inductor

Increased loss will result in a low-Q inductor which associate drawback to RFIC circuit as described below.

- Increased phase noise in oscillators
- High insertion loss in filters & baluns
- High power consumption in amplifiers
- Poor I/O impedance matching

So, the loss is important factor in design of inductor and should be taken care. Figure 2 shoows the lumped model of inductor with more relaistic way different than simple model.



Fig. 2 Lumped Model & on-chip inductor model

Ls is desired Inductance value, Rs metal sheet resistance, Cs series feed-forward capacitance or sum of all overlap capacitance, Cox spiral to substrate capacitance, Csi Substrate capacitance, Rsi substrate resistance.

R1 & L1 are Eddy current components, skin effects, proximity effects :

- On substrate
- On metal trace

Eddy Currents:

Eddy current can be excited on substrate and on metal trace. skin effect is the tendency of an alternating electric current (AC) to become distributed within a conductor such that the current density is largest near the surface of the conductor, and decreases with greater depths in the conductor. The electric current flows mainly at the "skin" of the conductor, between the outer surface and a level called the skin depth. The skin effect causes the effective resistance of the conductor to increase at higher frequencies where the skin depth is smaller, thus reducing the effective cross-section of the conductor. The skin effect is due to opposing eddy currents induced by the changing magnetic field resulting from the alternating current. At 60 Hz in copper, the skin depth is about 8.5 mm. At high frequencies the skin depth becomes much smaller. Increased AC resistance due to the skin effect can be mitigated by using specially woven litz wire.



Fig. 3 Skin depth is due to the circulating eddy currents (arising from a changing H field) cancelling the current flow in the center of a conductor and reinforcing it in the skin.

Penetration depth can be expressed as:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}.$$

Skin effect comes from inhomogenous current density due to magnetic field of single conductor that increases the resistance resistance. Proximity effect is similar to skin effect, but it is due to field from adjacent conductors. Eddy current also become excited inside the substrate. This effects will result in incressed Rs & Substrate loss.





Fig. 1. Schematic view of a spiral inductor with substrate losses.

Fig. 4 Eddy Current on metal and inside the Substrate

Spiral Inductor Lumped Modeling:

Spiral inductor lumped model can be simplified as shown below.



Fig. 5 Simplified lumped model of spiral inductor

$$R_{p} = \frac{1}{\omega^{2} C_{ox1}^{2} R_{sb1}} + \frac{R_{sb1} (C_{ox1} + C_{sb1})^{2}}{C_{ox1}^{2}}$$
$$C_{p} = C_{ox1} \cdot \frac{1 + \omega^{2} (C_{ox1} + C_{sb1}) C_{sb1} R_{sb1}^{2}}{1 + \omega^{2} (C_{ox1} + C_{sb1})^{2} R_{sb1}^{2}}$$

For quality factor we can write:

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}$$

$$Q = \frac{\omega L}{R_s} \cdot \frac{R_p}{R_p + \left[\left(\frac{\omega L}{R_s} \right)^2 + 1 \right] R_s} \cdot \left[1 - \frac{R_s^2 (C_{cp} + C_p)}{L} - \omega^2 L (C_{cp} + C_p) \right]$$
$$Q = \frac{\omega L_s}{R_s} [\text{Substrate Loss Factor}] [\text{Self-resonance Factor}]$$
Maximum Attainable Q < 1 < 1

Q can be formulated as shownn above. So, based on the above relation some parameter can be changed to improve the quality factor including:

- Increase Rp
- Reduce Rs
- Reduce Cox
- Reduce Cs



Ways to improve Q:

High-Q integrated inductors are widely used to improve the performance of advanced RF integrated circuits such as voltage-controlled oscillators, low noise amplifiers, power amplifiers, mixers, filters and matching networks. The quality factor of on-chip inductors is limited by the loss mechanisms that convert the electromagnetic energy into heat. There are two separate sources of loss in inductors: the metal loss and the substrate loss. Therefore, the unloaded Q of an inductor can be expressed by :

$$\frac{1}{Q} = \frac{1}{Q_{\text{substrate}}} + \frac{1}{Q_{\text{metal}}}.$$

where Q substrate and Q metal represent the substrate loss and the Ohmic loss of metal strips, respectively. While metal loss can be reduced by using thick high-conductivity metals, the loss of Si substrate has remained the major barrier in reaching Q 's comparable to that of offchip inductors. Micromachining techniques have been utilized to improve the Q substrate . Approaches taken to reduce the substrate loss and increase the Q can be summarized as the use of a thick insulating layer, whether by suspension of the inductor or by the use of a thick dielectric. The substrate loss is known to decrease with increasing thickness of the insulating layer. However, there is a saturation thickness for the dielectric beyond which the Q remains constant. On the other hand, the electromagnetic field produced by the current flowing in the inductor vanishes in the close vicinity of the edge of the inductor (tens of microns), resulting in saturation behavior for the inductor Q versus the area of the insulating layer. This is of special importance when an upper limit exists on the area of the insulating layer due to the processing constraints.

There are various ways to improve the Q of inductor based on conducted studies and can be summarized as follow.

- Physical Properties (width, spacing...)
- Patterned Ground Shield (PGS)
- Metal Stack, Thicker Metal Layer
- High Resistivity Substrates
- New inductor models
- Oxide Etching

1-High Resistivity Substrate [2]

Substrate can be changed to a one with high resistivity. There are high resistivity substrates like Glass (with relative permitivity: 5-6) which can replace the Silicon and this way we are going to have:

- high Rsub (compared to Si)
- Reduced Csub (compared to Si)

Impedance of the substrate network simply reduces to a single capacitance dominated by the smaller between Cox and Csub



2-Polymer Cavity [15]

In this method a part of substrate can be replaced by polymer. Doing so, we have:

- Increase Rp (Rsub)
- Reduce Cp (Csub+Cox)
- Polymer underneath (perm:2.75)
 - Higher resistivity (\rightarrow high Rp)
 - Lower permitivity (\rightarrow low Cp)

$$Q = \frac{\omega L}{R_s} \frac{R_p}{\left[\left(\frac{\omega L}{R_s}\right)^2 + 1\right]R_s} \cdot \left[1 - \frac{R_s^2(C_{cp} + C_p)}{L} - \omega^2 L(C_{cp} + C_p)\right]$$



3-Change Model [10]

The model of inductor can be changed in way that reduce the mutual coupling between the adjacent current element.

A model shows below modify the series feed-forward capacitance or sum of all overlap capacitance, metal to metal cap, Cs.



4-Oxide Etching [4]

Remove the oxide layer between the spiral and substrate by an optimized etching tech.



- Improve the insulation to inductor
- Relative permitivity becomes 1 (vacuum)
- Cox capacitance minimized
- Reduced substrate effect

5-Metal Thickness & Stack [18]

Physical Properties (width, spacing...) of the metal can be changed in a way to improve the quality factor as shown below.

- Increase metal thickness for high-Q :
 - Increased metal sidewall areas of current
 - Decreased metal resistance, Rs
- Stack the metals :
 - Combine metal layers through vias
 - Decreased metal resistance, Rs





3

Frequency(GHz)

4

2

5

6-Patterned Groung Shielding [9]

Ground plane can be changed in a way to reduce the effect of eddy current.

- Substrate Loss Factor approaches to unity as $Rp \rightarrow inf$.
- Rp approaches to inf. as $Rsi \rightarrow inf. \text{ or } Rsi \rightarrow 0$.
- Patterned Groung Shielding acts as a short.
- Slotted pattern reduces the negative mutual coupling. The slots act as open circuit. Prevents the build up of image current

$$Q = \frac{\omega L}{R_s} \frac{R_p}{\left[\left(\frac{\omega L}{R_s}\right)^2 + 1\right]R_s} \cdot \left[1 - \frac{R_s^2(C_{cp} + C_p)}{L} - \omega^2 L(C_{cp} + C_p)\right]$$



